

**Maxfield Parson-Scherban**  
School of Engineering and Applied Sciences (SEAS)  
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**Education**

**Columbia University**

**PhD Expected May 2028**, 3.998

Electrical Engineering with a focus in motor control and power electronics

**Columbia University**

**Master of Science February 2025**, 3.72

Electrical Engineering with a focus in power electronics and circuit design

**Columbia University**

**Bachelor of Science May 2023**, 3.67

Electrical Engineering with a focus in power electronics and circuit design

**SKILLS**

Programming: Matlab, Python, Java, C, Verilog, System Verilog

CAD and Simulation: Cadence, KiCad, Virtuoso, LTSpice

Language: English (native)

Other: LaTeX, Linux Kernel, Circuit Analysis and Design

**WORK EXPERIENCE**

**MPLAB Research Laboratory**

**Motor Optimization Researcher** May 2023 - Present

- Increased speed of WRSM motor efficiency optimization problem code by over 700% leveraging applied math techniques such as semidefinite relaxation
- Analyzed Existing MATLAB code modeling efficiency of WRSM motor. Strategized combining FEA and PWA techniques
- Reviewed and analyzed relevant mathematics including SDP optimization technique. Studied relevant material and papers on history of motor optimization as well as current projects. PMSM paper led to personal goal of improving efficiency of WRSM by 2% from current industry standard

**Columbia University**

**Smart Energy and Storage TA** September 2023 - Present

- Provided support for Dr. Mohamad Kamaludeen in his Battery Energy Storage and Renewable Energy classes in the Engineering Department
- Facilitated guest lectures with energy industry experts ranging from national lab researchers to utility executives

**ELECTRICAL ENGINEERING PROJECTS**

**FSAE: Tractive System Active Light** Sep 2021 - May 2023 • Designed, tested, and fabricated 6 versions of tractive system active light from simulation to PCB layout using Kicad and LTSpice.

**Senior Design Expo: Uninterruptible Power Supply** Sep 2022 - May 2023 • Designed, tested, and fabricated 2 versions of uninterruptible power supply from simulation to PCB layout using Kicad and LTSpice.

**Digital VLSI Circuits: 8-bit CPU** Sep 2022 - Dec 2022 • Implemented Cadence, Virtuoso, Questasim, and ADE L to design and test 8-bit CPU layout in 90nm node • Partnered with another student to simultaneously design 7 components of the CPU.

**INTERESTS** - HAM radio, Pinball, Card Games, Fencing, Traveling